## REMARKS

Thorough examination and careful review of the application by the Examiner is noted and appreciated.

Claims 1-16 are pending in the application. Claims 1-16 stand rejected.

### Claim Rejections Under 35 USC §102

Claims 1-3, 5-12 and 14-16 are rejected under 35 USC §102(b) as being anticipated by Noguchi et al '610. It is contended that, regarding claim 1, Fig. 23 of Noguchi discloses a MOS device comprising: a semiconducting substrate 31 having source and drain regions 33; a gate dielectric layer 40 of less than 100 angstroms thickness (col. 24, lines 58-60) on the semiconducting substrate 31; and a gate 41 formed of Pt (col. 46, lines 47-51) on to of the dielectric layer 40.

The rejection of claims 1-3, 5-12 and 14-16 under 35 USC §102(b) based on Noguchi et al is respectfully traversed.

Noguchi et al '610 discloses "a semiconductor device comprises a chip including a **MISFET** having a source and a drain, in which one of the source and the drain is connected to a second current supply node ...". The Applicants respectfully submit that Noguchi et al discloses a MISFET device, not a MOSFET device as **disclosed and claimed** by the present invention independent claim 1:

> "Claim 1. A **metal oxide semiconductor (MOS)** device comprising:
>
> a semi-conducting substrate having source and drain regions;
>
> a gate dielectric layer of less than 100 Å thickness on said semi-conducting substrate; and
>
> a gate formed of a metal selected from the group consisting of Re, Rh, Ir and Ru on top of said gate dielectric layer."

The present invention does not recite a MISFET device.

Moreover, Fig. 23 of Noguchi et al in showing a MISFET device, shows a gate electrode 41 formed on top of a gate insulation film 40. As recited in col. 23, lines 57-61:

> "In the present embodiment, an element structure shown in Fig. 23 may be used to realize the circuit structure shown in, e.g., Fig. 19A. In Fig. 23, **a gate electrode 41 having e.g., polysilicon to which a B or P dopant is added** is formed through a gate insulation film 40 having, e.g., silicon oxide ..."

The gate electrode 41 shown in Fig. 23 by Noguchi et al is therefore not formed of Pt, as contended by the Examiner, instead, it is formed of polysilicon. Regarding the citation of col. 46, lines 47-51 by the Examiner, the recitation refers to, not Fig. 23, but instead Fig. 47, for a gate electrode 127 in a MISFET device. None of the elements recited in independent claims 1 and 10 of the present invention, i.e. Re, Rh, Ir and Ru, is disclosed by Noguchi et al, at col. 46, lines 47-51.

The rejection of claims 1-3, 5-12 and 14-16 under 35 USC §102(b) based on Noguchi et al is respectfully traversed. A reconsideration for allowance of these claims is respectfully requested of the Examiner.

Claims 1-4 and 6-15 are rejected under 35 USC §102(e) as being anticipated by Maria et al. It is contended that, regarding claim 1, Fig. 4 of Marie et al discloses a MOS device including a semiconducting substrate 16 having a gate dielectric layer 20''' of less than 100 angstroms thick on the substrate, and a gate 22 formed of Pt on top of the dielectric layer 20'''.

The rejection of claims 1-4 and 6-15 under 35 USC §102(e) based on Marie et al is respectfully traversed.

In the newly amended independent claims 1 and 10, the metal used for forming the gate is limited to Re, Rh, Ir and Ru. None of such metals is disclosed or claimed by Maria et al. The only metallic component for the gate 22 disclosed by Marie et al is Pt. For instance, at page 3, paragraph 0034, it is disclosed:

> "In all of the embodiments of Figs. 1-4, the gate electrode may comprise doped polysilicon and preferably comprises a conductor, such as a metal. Preferred metals include platinum. Conventional gate electrode metals such as titanium nitride and aluminum preferably are not used ..."

The rejection of claims 1-4 and 6-15 under 35 USC §102(e) based on Marie et al is respectfully traversed. A reconsideration for allowance of these claims is respectfully requested of the Examiner.

Based on the foregoing, the Applicants respectfully submit that all of the pending claims, i.e. claims 1-16, are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version With Markings To Show Changes Made".

In the event that the present invention is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**In The Claims**

Claim 1 has been amended as follows:

1. (Amended) A metal oxide semiconductor (MOS) device comprising:

a semi-conducting substrate having source and drain regions;

a gate dielectric layer of less than 100 Å thickness on said semi-conducting substrate; and

a gate formed of a metal selected from the group consisting of Re, Rh, Ir[, Pt] and Ru on top of said gate dielectric layer.

Claim 10 has been amended as follows:

10. (Amended) A field effect transistor (FET)comprising:

a semi-conducting substrate having at least one source and one drain region;

a gate dielectric layer of less than 100 Å thickness on the semi-conducting substrate; and

a gate formed of a metal selected from the group consisting of Re, Rh, Ir[, Pt] and Ru on top of the gate dielectric layer.